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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/681,399	10/08/2003	Yuanning Chen	TI-35212	7440

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TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
FARAHANI, DANA	
ART UNIT	**PAPER NUMBER**
2891	

DATE MAILED: 05/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/681,399	CHEN ET AL.	
	Examiner	Art Unit	
	Dana Farahani	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/08/3*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 3, 7, and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Hong et al., hereinafter Hong (US Patent 5,457,061).

Regarding claims 1, 3, and 7, Hong discloses in figures 3-6, a method of fabricating a semiconductor device, the method comprising:

forming a gate 38 on a semiconductor substrate, the gate including opposing side surfaces;

depositing an oxide material (SiO_2) 36 over the gate electrode and the semiconductor substrate, the opposing side surfaces of the gate being substantially free of the oxide material; and

forming spacers 40 on the opposing side surfaces of the gate, the spacers contacting the opposing side surfaces of the gate substantially along the opposing side surfaces.

Regarding claim 8, Hong discloses providing a nitride layer over the gate after depositing the oxide material; and

etching the nitride layer (see column 4, lines 5-10).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2, 12, 13, 16, 17, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hong as applied to claim 1 above, and further in view of Reisinger (US Patent 6,137,718).

Hong discloses the claimed invention, as discussed above, except for the gate being doped.

Reisinger discloses a memory transistor with a gate that is n-doped polysilicon, as an alternative to a metal gate (see column 5, lines 57-63). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to dope the gate in the device of the Hong's structure, since doped (semiconductor) gates and conductor gates are alternatively used in MOS transistors. Although Hong in view of Reisinger does not disclose the gate is p-type dopant (claim 17) and the transistor is p-type (claim 19), it would have been obvious to one of ordinary skill in the art at the time of the invention to switch from NMOS transistor to a PMOS transistor, and n-type dopant to p-type dopant in accordance with one of ordinary skill in the art preference of having holes as the majority carriers in the device.

5. Claims 4-6, 14, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hong, and Hong in view of Reisinger, in case of claims 14 and 15, as applied to claims 1 and 12 above, and further in view of Jeng (US Patent 6,303,490).

Hong, and Hong in view of Reisinger discloses the claimed invention, as discussed above, except for an anisotropic Physical Vapor Deposition (PVD) which comprises one of collimated sputtering, long throw sputtering or ionized metal plasma method is used in depositing the oxide material.

Jeng discloses anisotropic ionized metal plasma sputtering method is used for deposition which gives a good surface coverage (see column 4, lines 24-28). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use this method to deposit the oxide layer of the Hong reference, since the advantage of using the method is known in the art.

6. Claims 9, 10 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hong, and Hong in view of Reisinger, in case of claim 18, as applied to claims 8 and 12 above, and further in view of Nishimoto et al., hereinafter Nishimoto (US Patent 5,814,543).

Hong, and Hong in view of Reisinger discloses the claimed invention, as discussed above, further disclosing forming source and drain regions 42 and 52, but does not disclose implanting an LDD implant after forming the gate, but before depositing the oxide layer.

Nishimoto discloses in figure 20 a memory circuitry, which implements LDD regions 6. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to from LDD regions in the memory unit of the Hong reference in order to make it usable in a memory circuitry, which require LDD regions. Note that although Hong in view of

Nishimoto does not disclose the LDD regions are formed after forming the gate but before depositing the oxide layer, it would have been obvious to one of ordinary skill in the art at the time of the invention to determine the order of forming these regions, according to the manufacturing environment and convenience of one of ordinary skill in the art. See *Ex Parte Rubin* 126 USPQ 440 (BAPI 1959) for the proposition that reversing the order of a process sequence cannot be considered an act of invention.

7. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hong.

Hong discloses the claimed invention, as discussed above, except for expressly disclosing the transistor is PMOS. However, it would have been obvious to one of ordinary skill in the art at the time of the invention to switch from NMOS transistor to a PMOS transistor in accordance to one of ordinary skill in the art preference of having holes as the majority carriers in the device.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dana Farahani whose telephone number is (571)272-1706. The examiner can normally be reached on M-F 9:00AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on (571)272-1722. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

D. Farahani

B. WILLIAM BAUMEISTER
SUPERVISORY PATENT EXAMINER